

Myna II

Project code: 91.4C201.001

PCB REVISION: 05216-SB

CLK GEN.
IDT CV125

3

Mobile CPU
Dothan

CLE-1.5G / Dothan2.13G
(CPU on board,no socket)

4, 5

G792

19

HOST BUS 533MHz

DDR II
400/533 MHz

11,12

400/533MHz

Alviso-GM

KI.91501.017

400/533MHz

DDR II
400/533 MHz

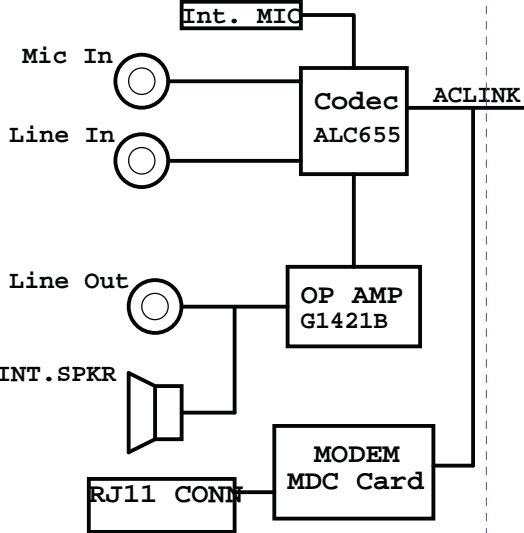
11,12

6,7,8,9,10

DMI I/F 100MHz

ICH6-M

Ver.: B2, KI.80101.011



IO Board

(co-lay with PCMCIA)

New card

29

PWR SW
TPS2231

29

PCI-E

PATA

two USB port
on IO Board

HDD

20

USB
3 PORT

21

MINI USB
Blue-tooth

21

IO Board

PCI BUS

LPC BUS

15,16,17,18

TI
PCI 7411
1* Slot Cardbus
1* 1394
CardReader

24,25

PCMCIA I/F

PCMCIA
SLOT
Support
TypeII

26

1394 6pin
Conn

MS/MS Pro/
xD/ MMC/SD
5 in 1

26

Mini-PCI
802.11A/B/G
(only smaller)

30

LAN
Giga
BCM5788-M

22, 23

TXFM

23

RJ45 CONN

23

NS
SIO
87392

31

KBC
Renesas RE144B

30

Touch
Pad

32

INT.
KB

32

BIOS ROM
4M BITS
PM49F004T-33VC

33

LPC
DEBUG
CONN.

33

SYSTEM DC/DC
TPS5130 41,42

| INPUTS | OUTPUTS |
|----------|---|
| DCBATOUT | 5V_S5 3V_S5 1D5V_S0 2D5V_S0(LDO) |

SYSTEM DC/DC
ISL6227 43

| INPUTS | OUTPUTS |
|----------|---------------------|
| DCBATOUT | 1D05V_S0 1D8V_S3 |

TPS51100DQG 43

| | |
|---------|--------------|
| 1D8V_S3 | VTT_S0(0.9V) |
|---------|--------------|

MAXIM CHARGER
MAX8725ETI 44

| INPUTS | OUTPUTS |
|----------|--|
| DCBATOUT | CHG_PWR 16.8V 3.2A UP+5V 5V 100mA |

CPU DC/DC
ISL6218CV-T 40

| INPUTS | OUTPUTS |
|----------|-------------------------------|
| DCBATOUT | VCC_CORE 0.844~1.3V 27A |

Easy Port 4 (124 PIN)

AC IN RJ45-11 SERIAL PORT CRT PRINTER PS2 MIC LINE IN LINE OUT TV OUT DVI PCIE X2 SMBUS

34, 35

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|----------------------------------|-----------------|-----|
| Title | BLOCK DIAGRAM | |
| Size Custom | Document Number | Rev |
| | Myna II | SB |
| Date: Monday, September 26, 2005 | Sheet 1 of 47 | |

Alviso Strapping Signals
and Configuration

page 7

| Pin Name | Strap Description | Configuration |
|---------------|-----------------------|---|
| CFG[2:0] | FSB Frequency Select | 000 = Reserved 001 = FSB533 010 = FSB800 011-111 = Reversed |
| CFG[3:4] | Reversed | |
| CFG5 | DMI x2 Select | 0 = DMI x2 1 = DMI x4 (Default) |
| CFG6 | DDR I / DDR II | 0 = DDR II 1 = DDR I |
| CFG7 | CPU Strap | 0 = Prescott 1 = Dothan (Default) |
| CFG[8:11] | Reversed | |
| CFG[12:13] | XOR/ALL Z test straps | 00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default) |
| CFG[14:15] | Reversed | |
| CFG16 | FSB Dynamic ODT | 0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default) |
| CFG17 | Reversed | |
| CFG18 | CPU core VCC Select | 0 = 1.05V (Default) 1 = 1.5V |
| CFG19 | CPU VTT Select | 0 = 1.05V (Default) 1 = 1.2V |
| CFG20 | Reversed | |
| SDVOCRTL_DATA | SDVO Present | 0 = No SDVO device present (Default) 1 = SDVO device present |

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

- 1.CHECK P5[1D5V & 1D5V-AVDD]
- 2.CHECK P8[PM & GM]

RESISTOR

| Symbol name | Value | Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %) | Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V | Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210 |
|-------------|----------|--|--|--|
| 10KR3 | 10K Ohm | If no letter, it means J: 5% | 1/16W, 75V | 0603 |
| 33D3R5 | 33.3 Ohm | If no letter, it means J: 5% | 1/10W, 100V | 0805 |
| 1KR3F | 1K Ohm | F: 1% | 1/16W, 75V | 0603 |

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

PCI Routing

| | IDSEL | IRQ | REQ/GNT |
|---------|-------|-------|---------|
| 7411 | 25 | B.F.G | 0 |
| MiniPCI | 21 | E | 1 |
| LAN | 23 | E | 2 |

CAPACITOR

| Symbol name | Value | Tolerance (M: +/-20, K: +/-10, Z: +80/-20) | Rating | Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210 |
|---------------|-------|---|--------|--|
| SCD1U10V2MX-1 | 0.1uF | M/X5R | 10V | 0402 |
| SC10U6D3V5MX | 10uF | M/X5R | 6.3V | 0805 |
| SC2D2U16V5ZY | 2.2uF | Z/Y5V | 16V | 0805 |

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceramic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

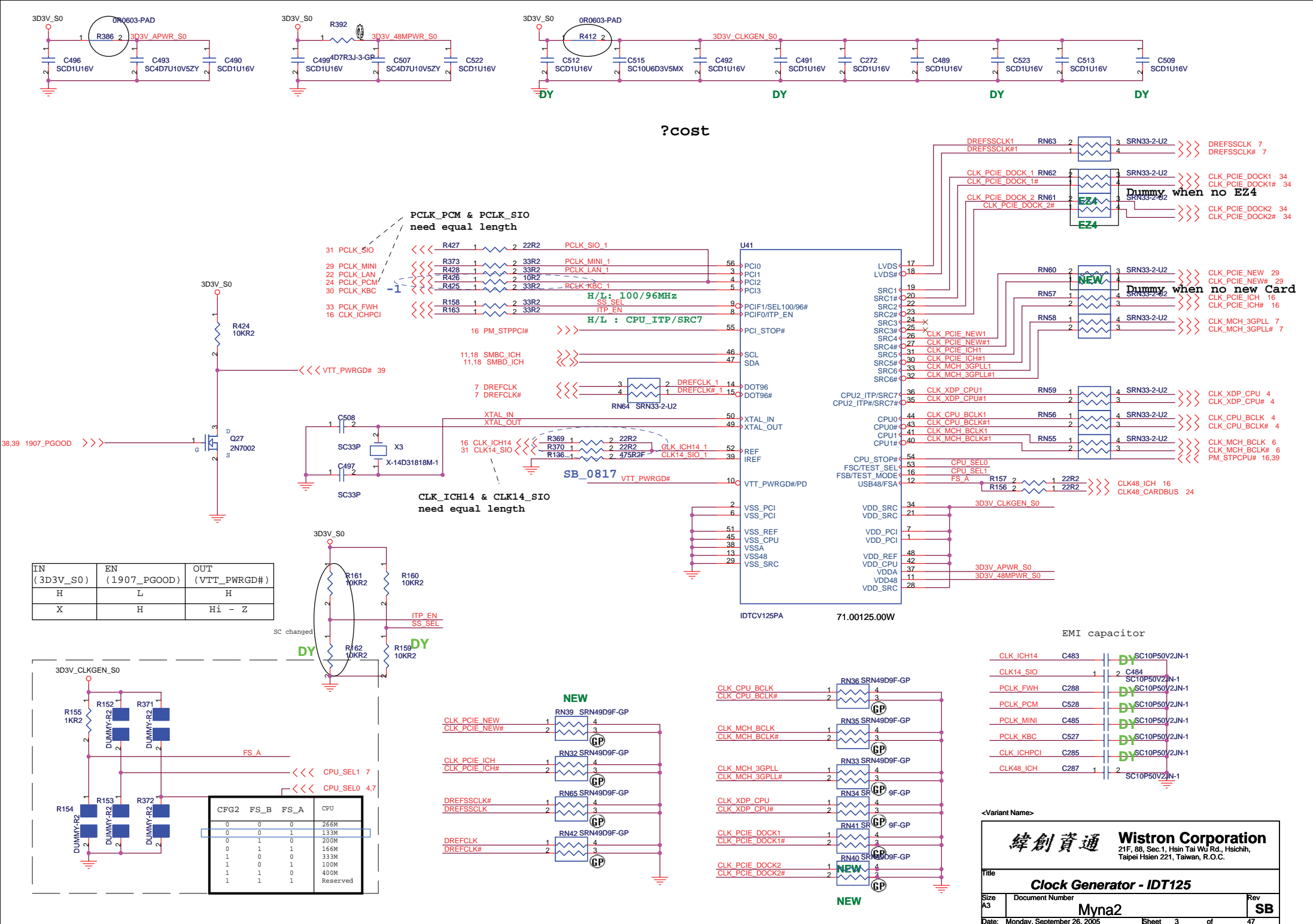
ICH6-M Integrated Pull-up
and Pull-down Resistors

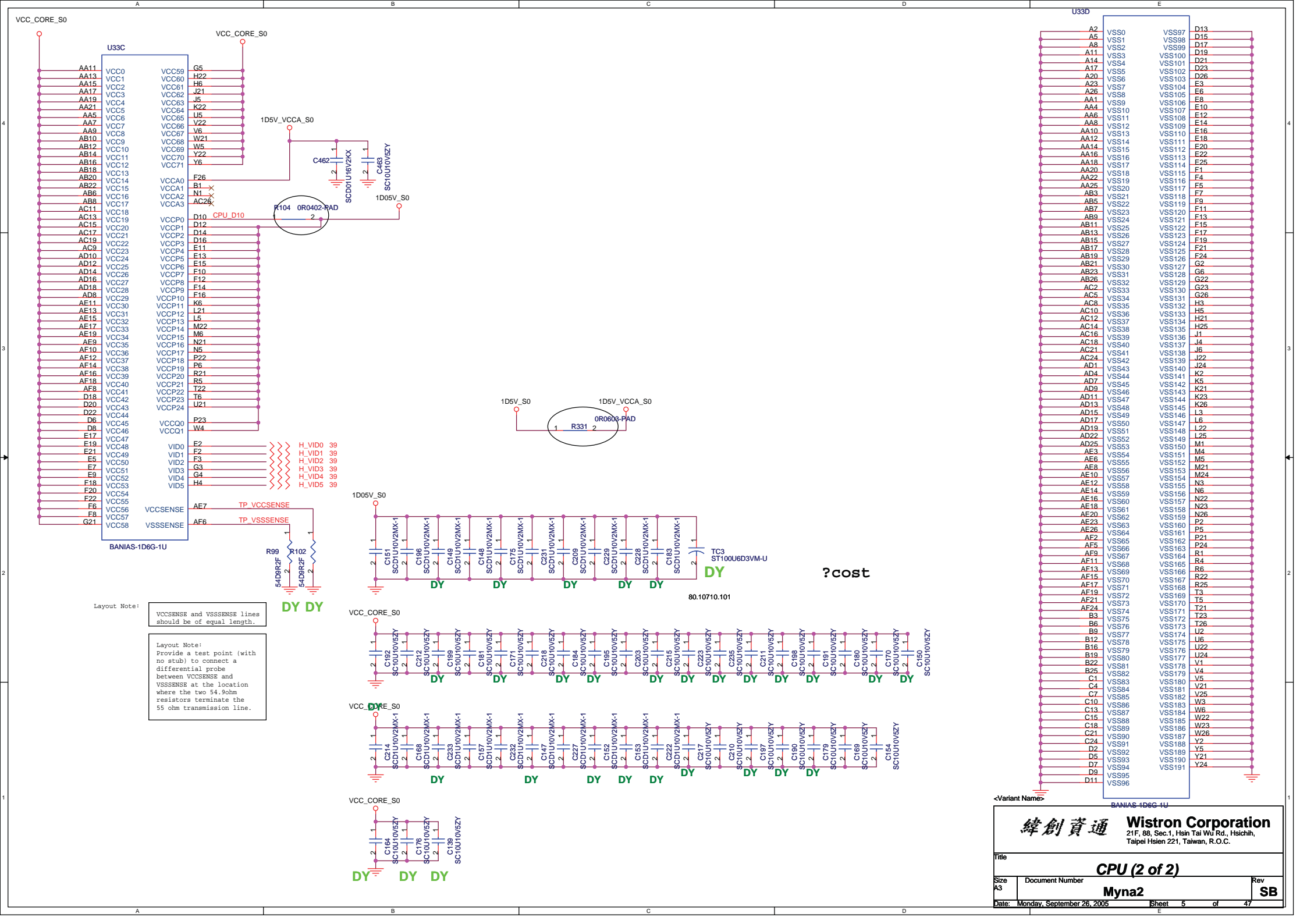
ICH6-M EDS 14308 0.8V1

| | |
|---|--------------------------------|
| ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3] | ICH6 internal 20K pull-ups |
| LAN_RXD[2:0] | ICH6 internal 10K pull-ups |
| ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT,ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS, | ICH6 internal 20K pull-downs |
| USB[7:0][P,N] | ICH6 internal 15K pull-downs |
| DD[7], SDDREQ | ICH6 internal 11.5K pull-downs |
| LAN_CLK | ICH6 internal 100K pull-downs |

ICH6-M IDE Integrated Series
Termination Resistors

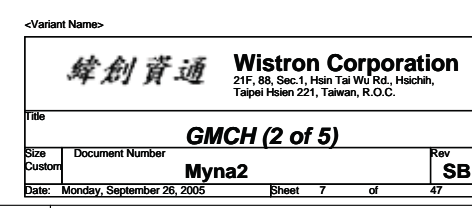
| | |
|--|----------------------|
| DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ | approximately 33 ohm |
|--|----------------------|

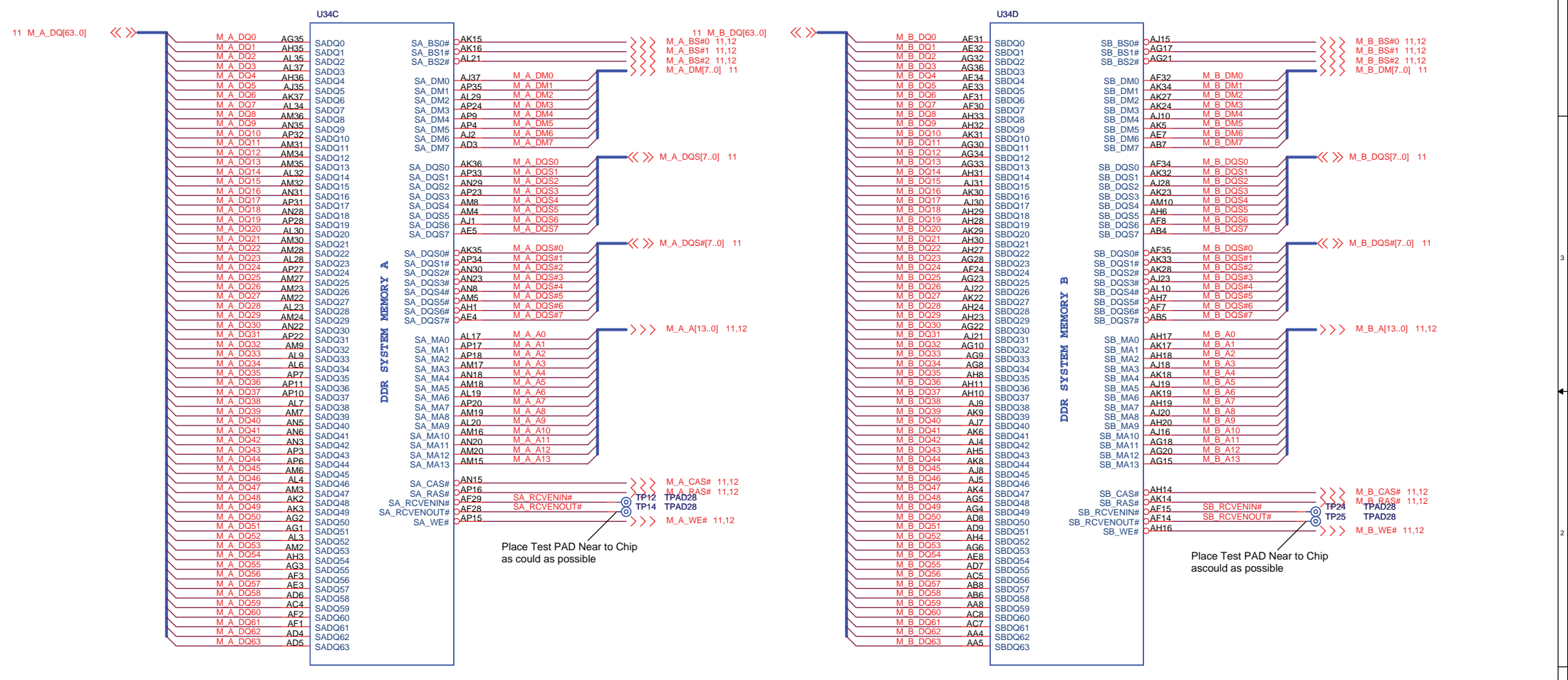






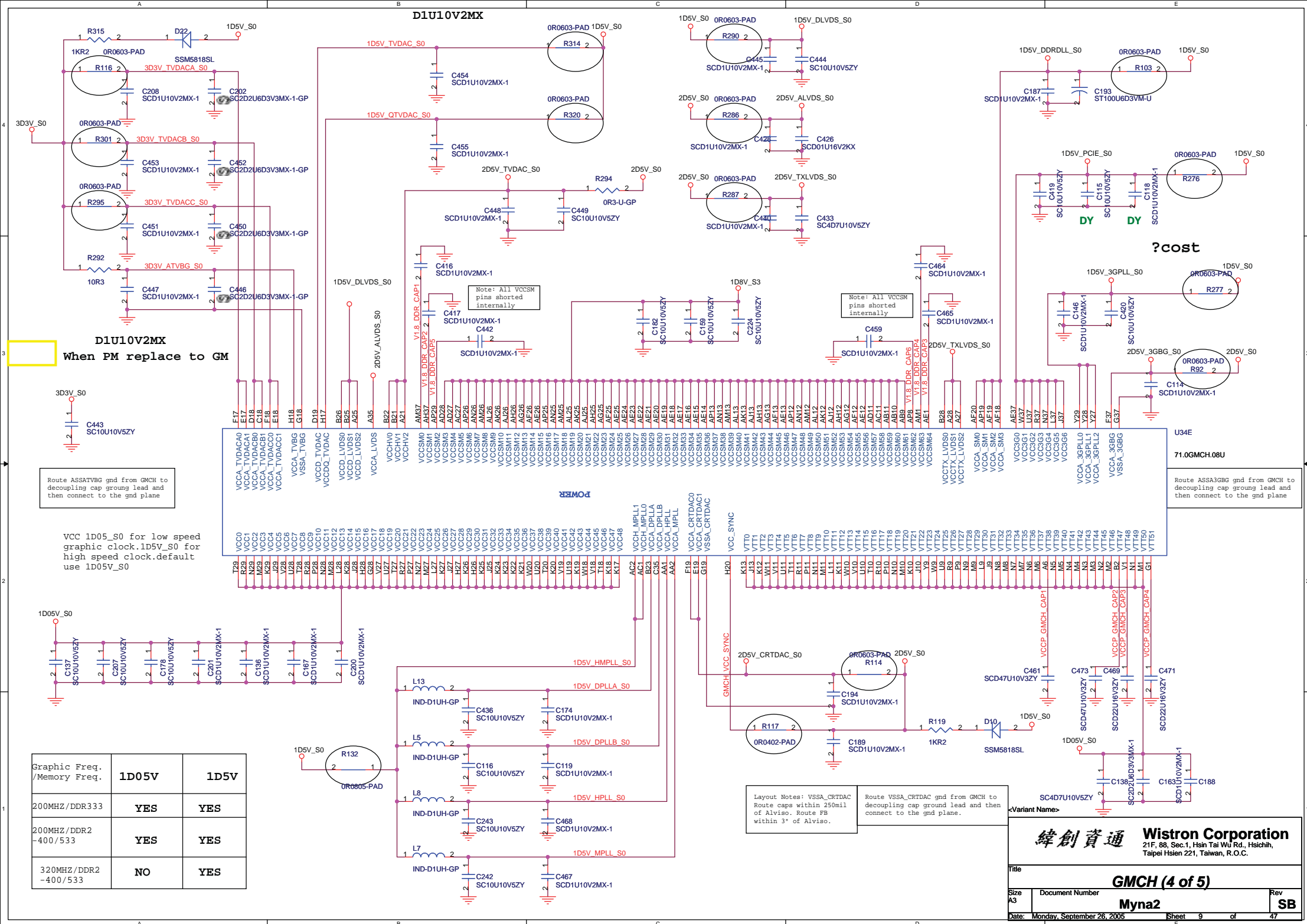
<Variant Name>

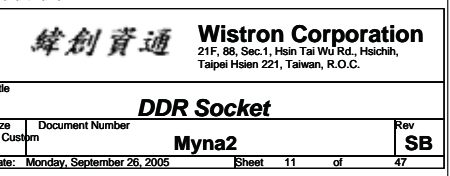




71.0GMCH.08U

71.0GMCH.08U





[illegible]

Put decap near power(0.9V)
and pull-up resistor

The diagram shows a PCB layout for the VTT_S0 signal. It features two rows of components connected by a horizontal bus. The top row includes capacitors C429, C427, C441, C430, C432, C434, C423, C421, and C422, all labeled SCD1U16V. The bottom row includes capacitors C438, C166, C173, C122, C125, C130, C127, C135, C133, C141, C131, C145, and C158, all labeled SCD1U16V. Pull-up resistors are indicated by green 'DY' labels at the beginning and end of the signal lines. A VTT_S0 input is shown at the top left.

10V_S3

Place these Caps near DM1

C132 SC2D2U6D3V3MX-1

C129 SC2D2U6D3V3MX-1

C140 SC2D2U6D3V3MX-1

C126 SC2D2U6D3V3MX-1

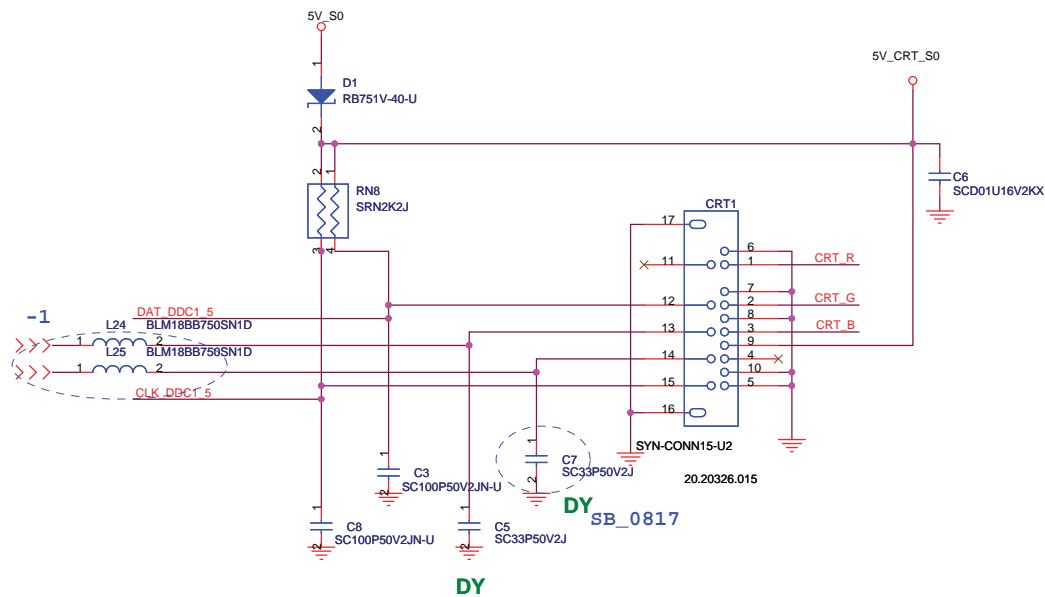
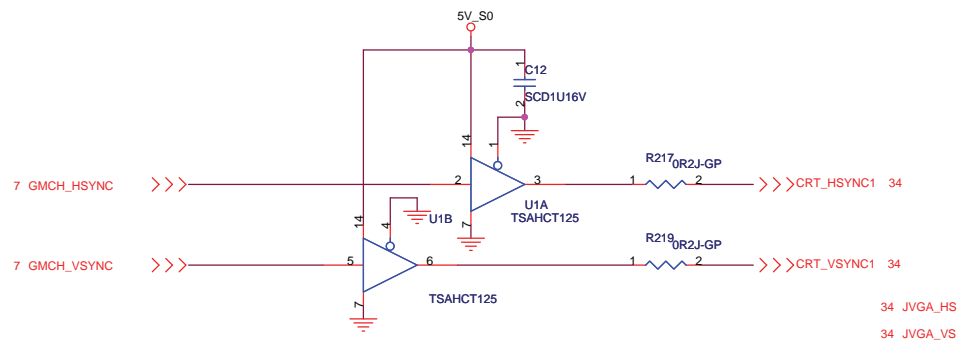
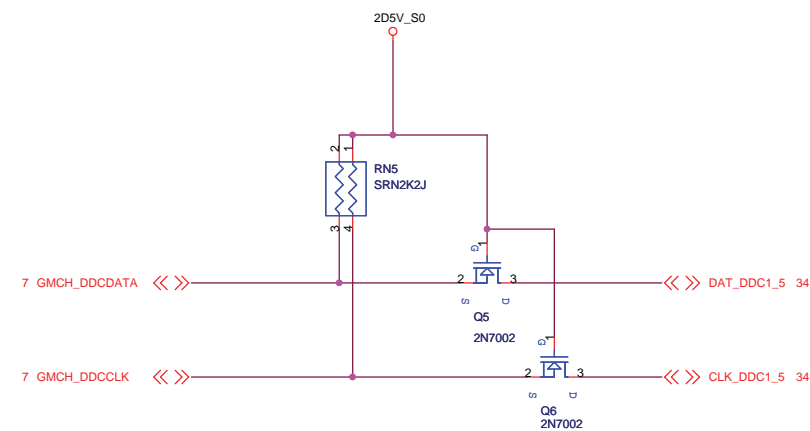
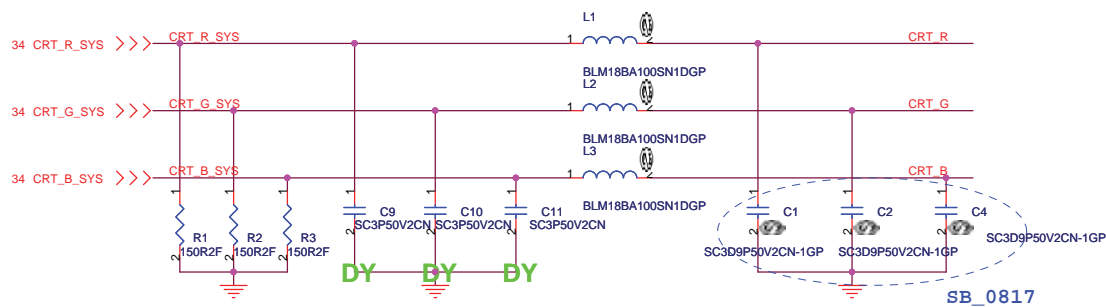
C123 10V

C143 10V

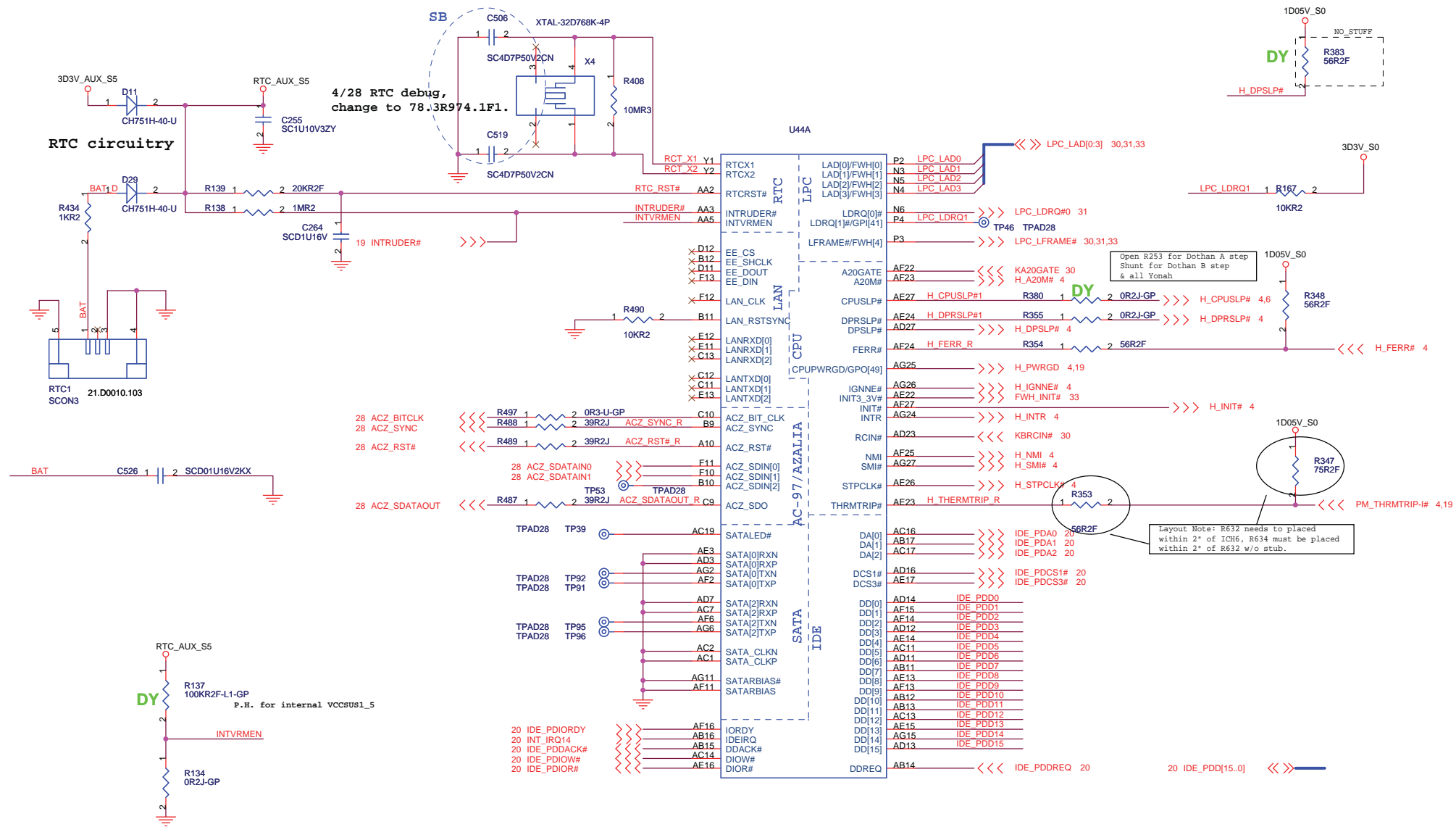
C120 10V

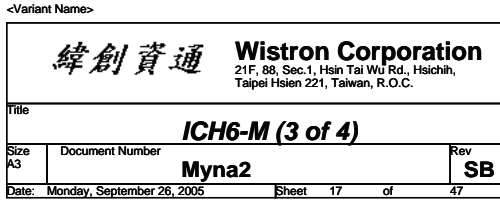
DM1

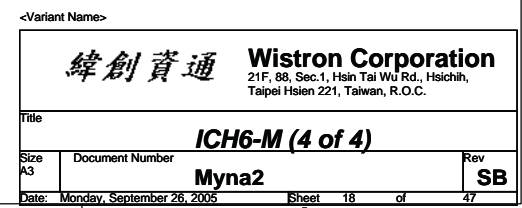
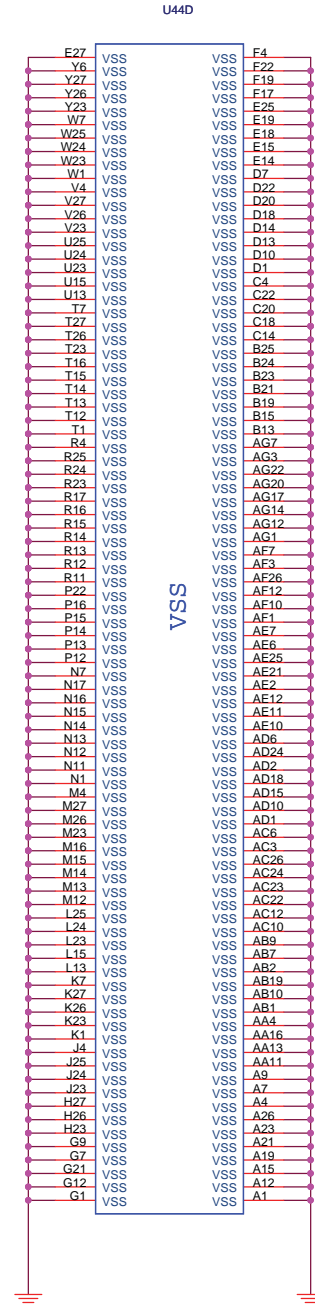
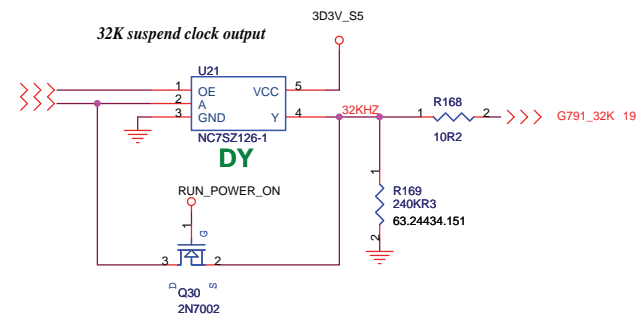
| | | | |
|----------------------------------|----------------------------|-------------|-----------|
| Title | | | |
| DDR2 Termination Resistor | | | |
| Size A3 | Document Number | | Rev |
| | Myna2 | | SB |
| Date: | Monday, September 26, 2005 | Sheet 12 of | 47 |

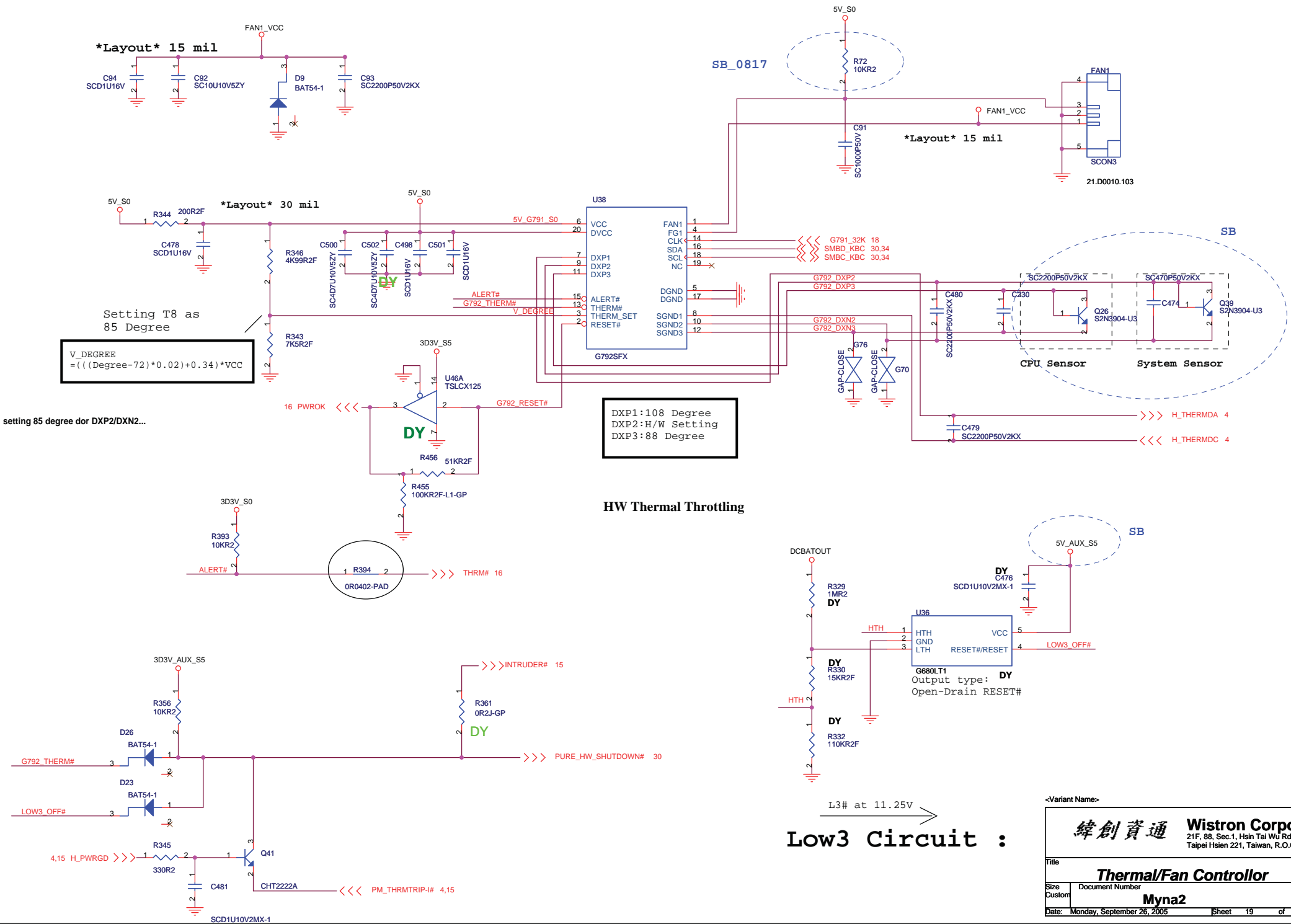


| | | | |
|---|----------------------------|-------|----------|
| <div> <div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div> </div> | | | |
| Title | | | |
| CRT Connector | | | |
| Size | Document Number | Rev | |
| A3 | Myna2 | SB | |
| Date: | Monday, September 26, 2005 | Sheet | 14 of 47 |

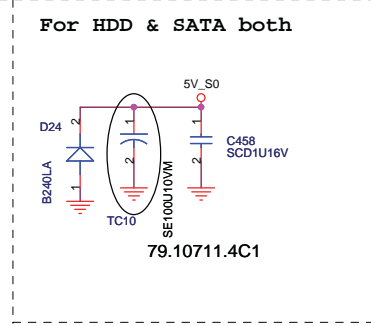








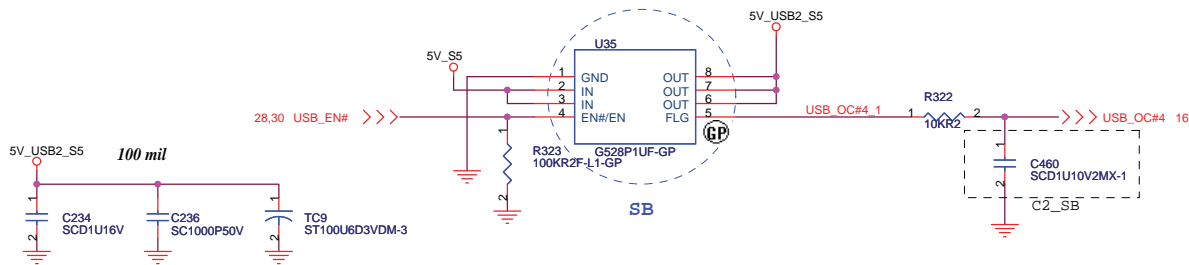
WWW.AliSaler.Com



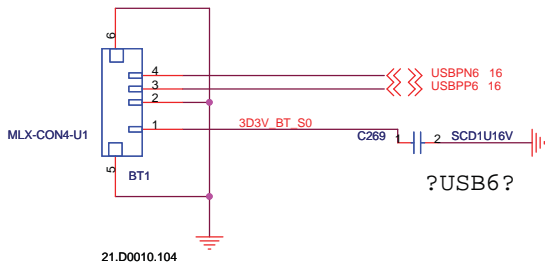
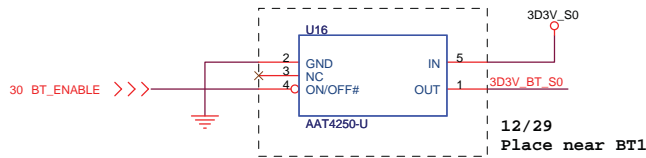
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Taipei Hsien 221, Taiwan, R.O.C.

| | | | |
|-----------------|----------------------------|----------|-------|
| Title | | | |
| PATA / SATA-HDD | | | |
| Size A3 | Document Number | | Rev |
| | Myna2 | | SB |
| Date: | Monday, September 26, 2005 | Sheet 20 | of 47 |

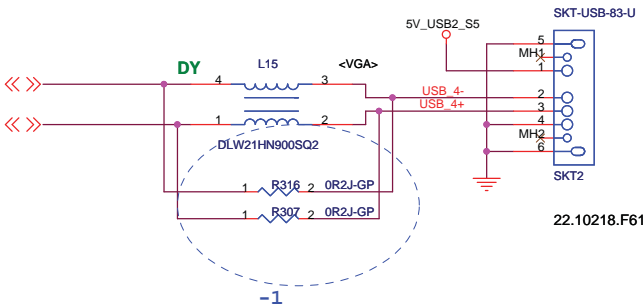
USB PORT



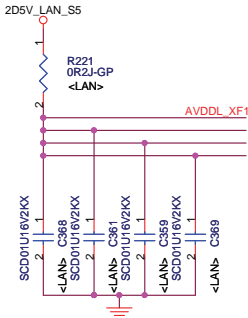
BLUETOOTH MODULE CONNECTOR



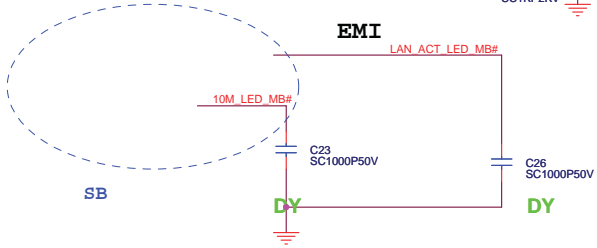
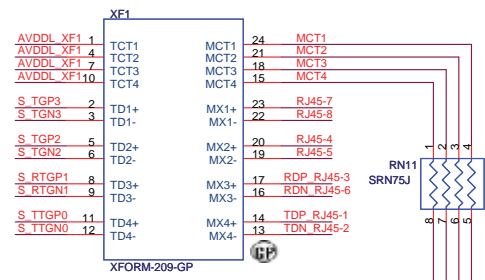
16 USBPN4
16 USBPP4







Giga Lan Transformer

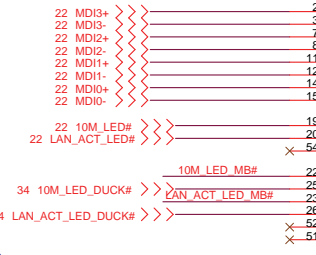


- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

Green LED: Speed 100: ON / Speed 10:OFF
Yellow LED: Link: ON, TX/RX:
Flash(10Hz).

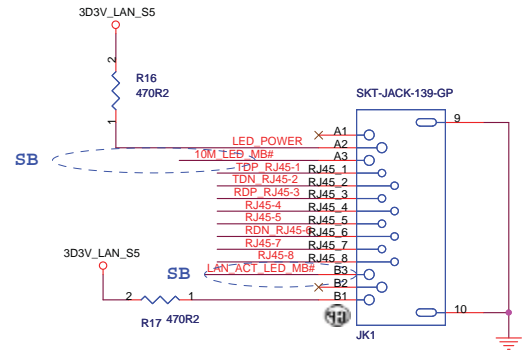
RJ11 signal must leave the other signal
or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers



| Function | SEL |
|-----------------|-----|
| An to nB1(MB) | L |
| An to nB2(DUCK) | H |

RJ45 Connector



Link: Green - 10Mbps/802.11b
Orange - 100Mbps/802.11a
Yellow - 1Gbps

<Variant Names>: Yellow

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Taipei Hsien 221, Taiwan, R.O.C.

Title

LAN Connector

Size

Document Number

Rev

Custom

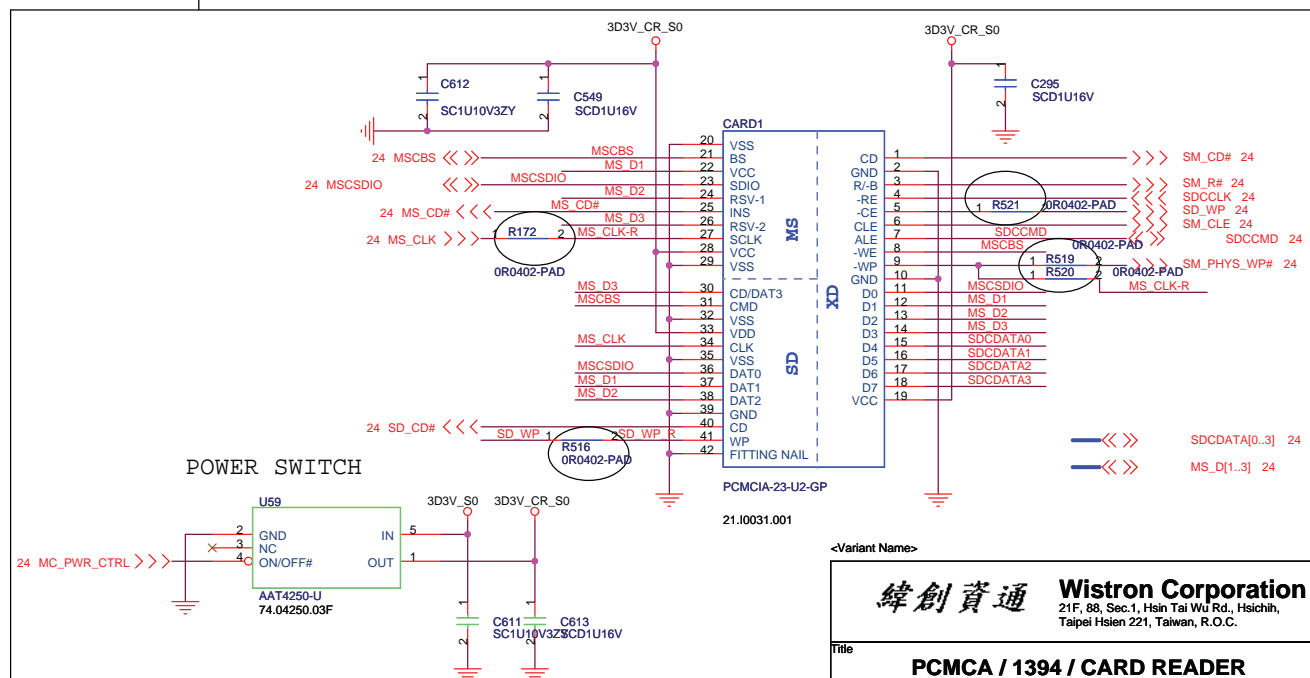
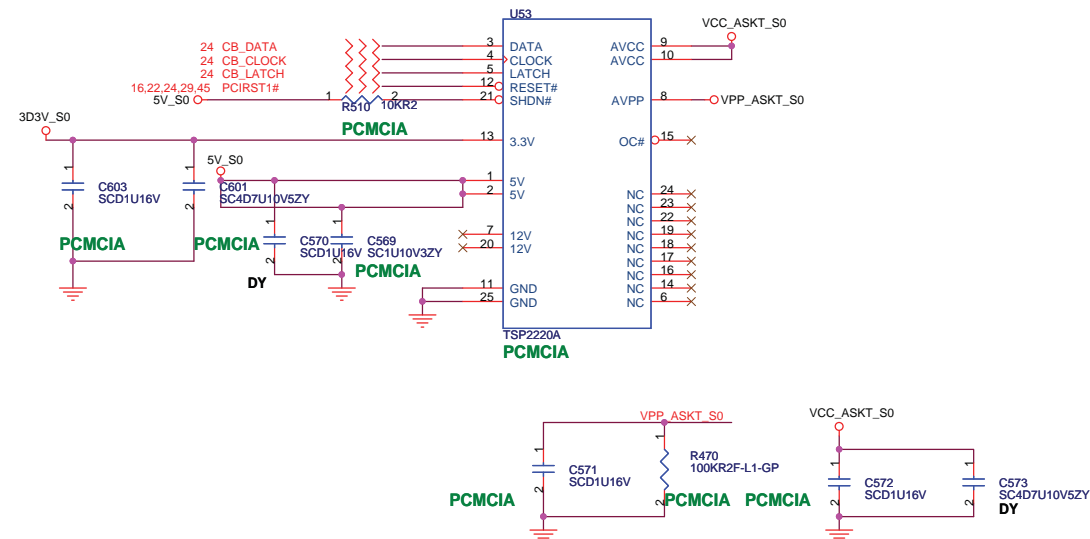
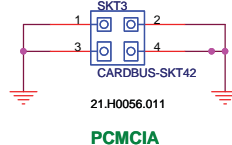
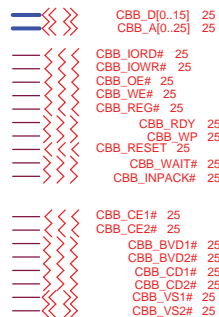
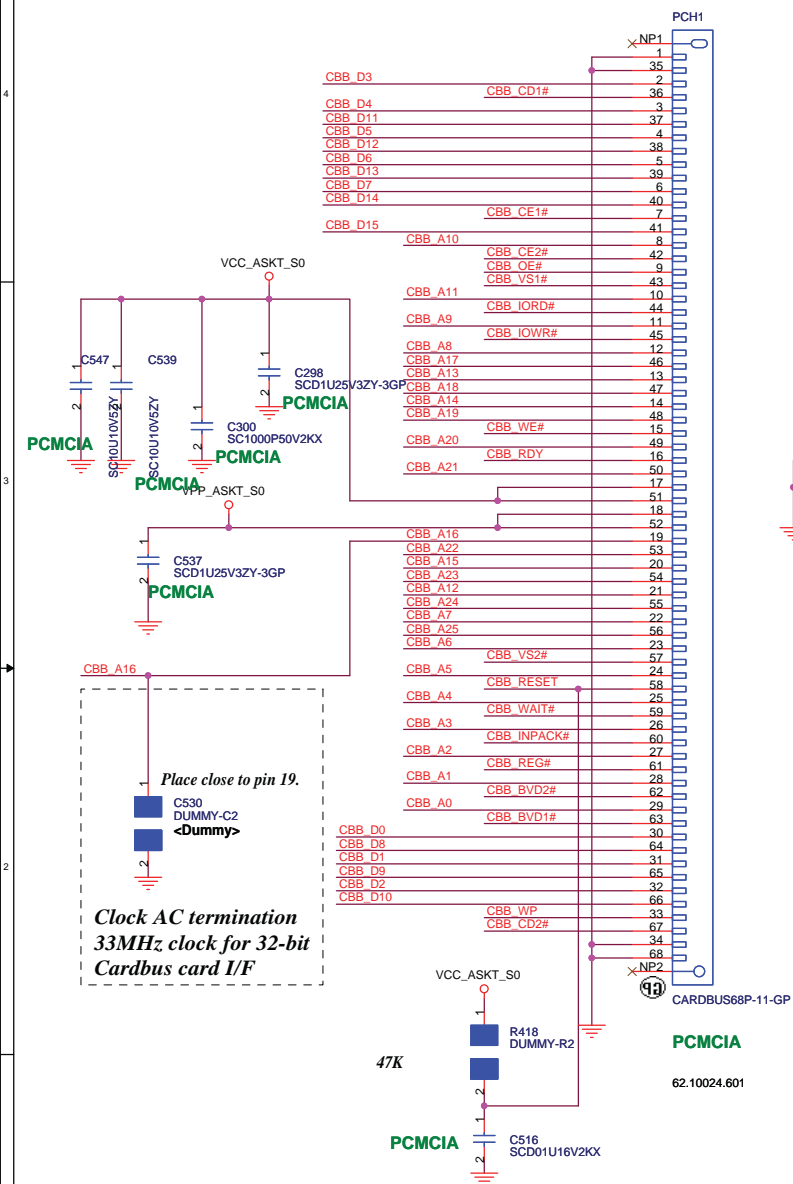
Myna2

SB

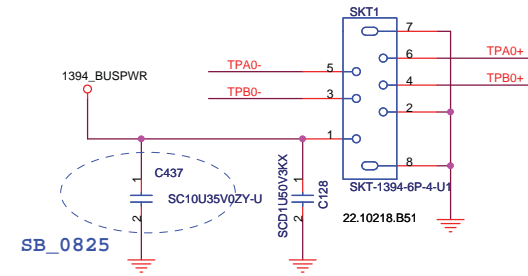
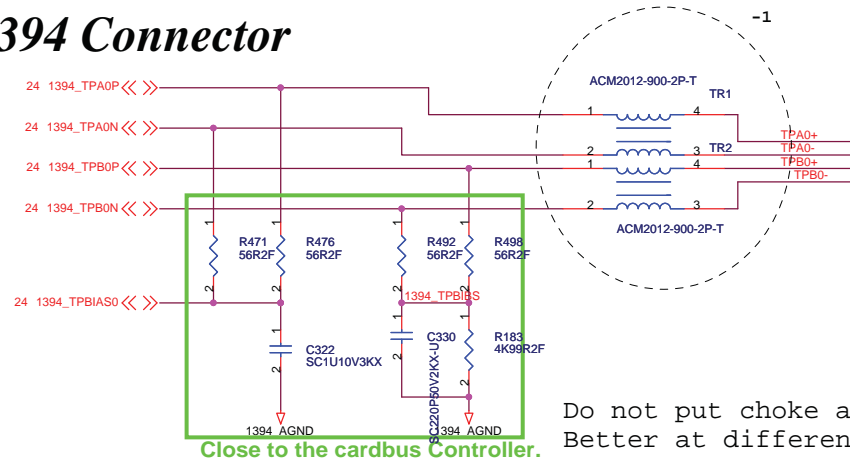
Date: Monday, September 26, 2006

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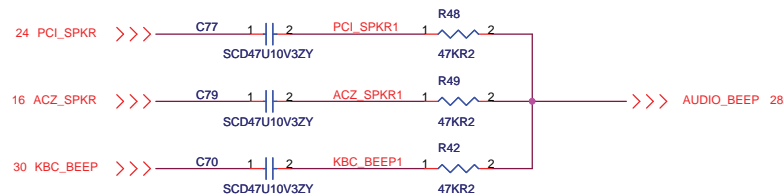
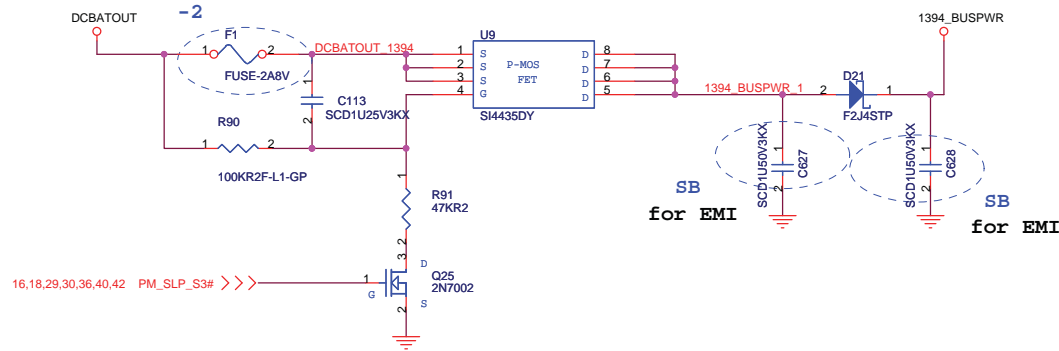
Power switch



1394 Connector



4/21 External ODD will suck more than 1.5A when battery mode

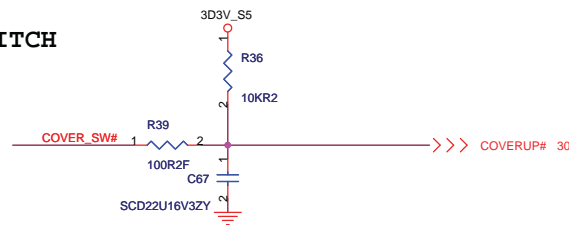


<Variant Name>

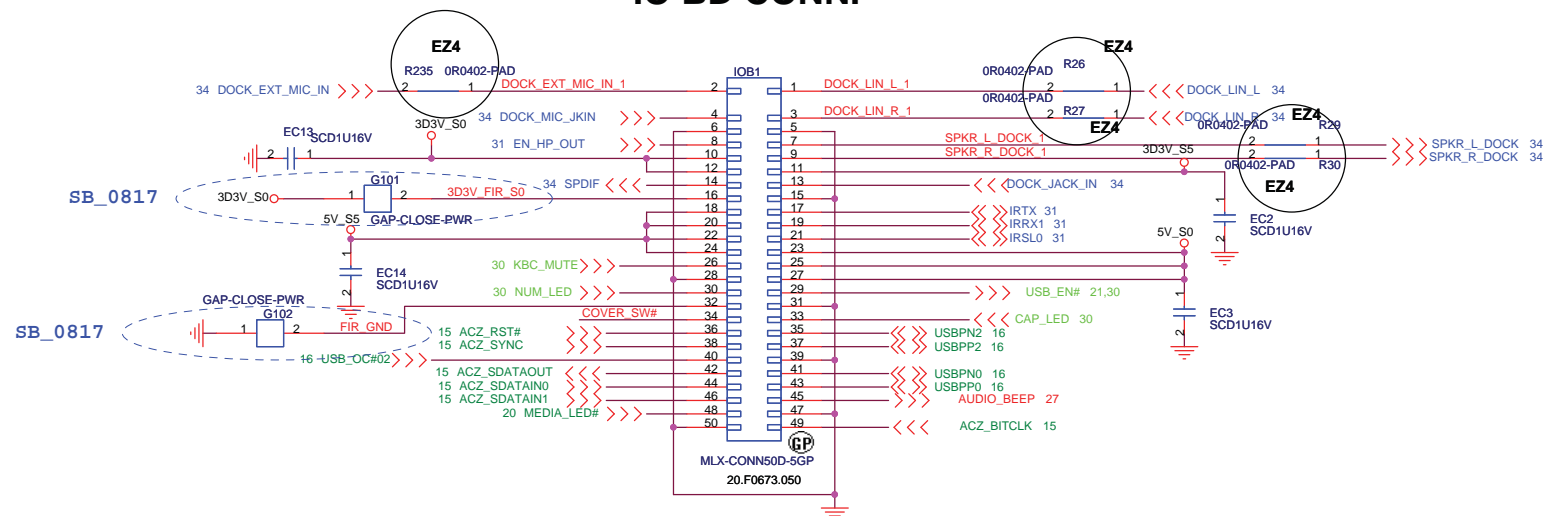
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| | | |
|----------------|----------------------------|----------------|
| Title | | |
| 1394 Connector | | |
| Size | Document Number | Rev |
| A3 | Myna2 | SB |
| Date: | Monday, September 26, 2005 | Sheet 27 of 47 |

COVER SWITCH



IO BD CONN.



Blue -> Dock or SuperIO
 Light Green -> KBC
 Green -> SouthBridge

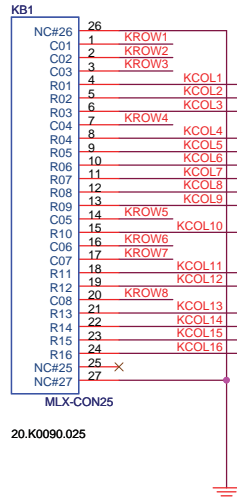
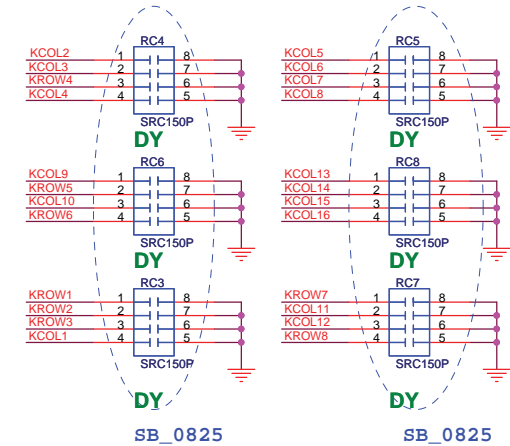
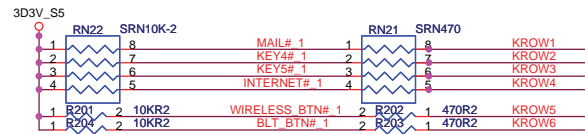
<Variant Name>

| | | | |
|----------------------------------|-----------------|---|-------|
| 緯創資通 | | Wistron Corporation | |
| | | 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | | | |
| AC'97 CODEC - ALC655 | | | |
| Size A3 | Document Number | Rev | |
| Myna2 | | SB | |
| Date: Monday, September 26, 2005 | | Sheet 28 | of 47 |

Launch BD CONN

Internal KeyBoard Connector

EMI CAPS

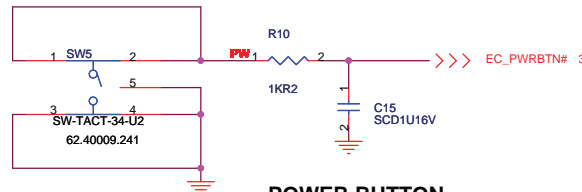
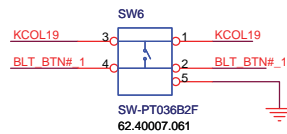
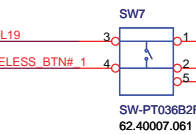
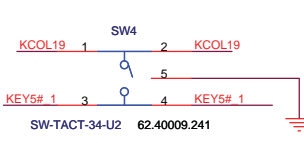
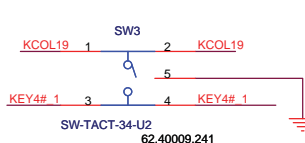
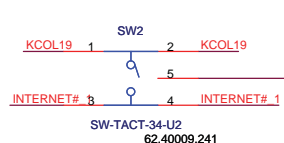
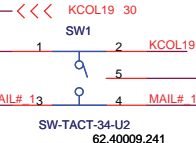


MAIL BUTTON

INTERNET BUTTON

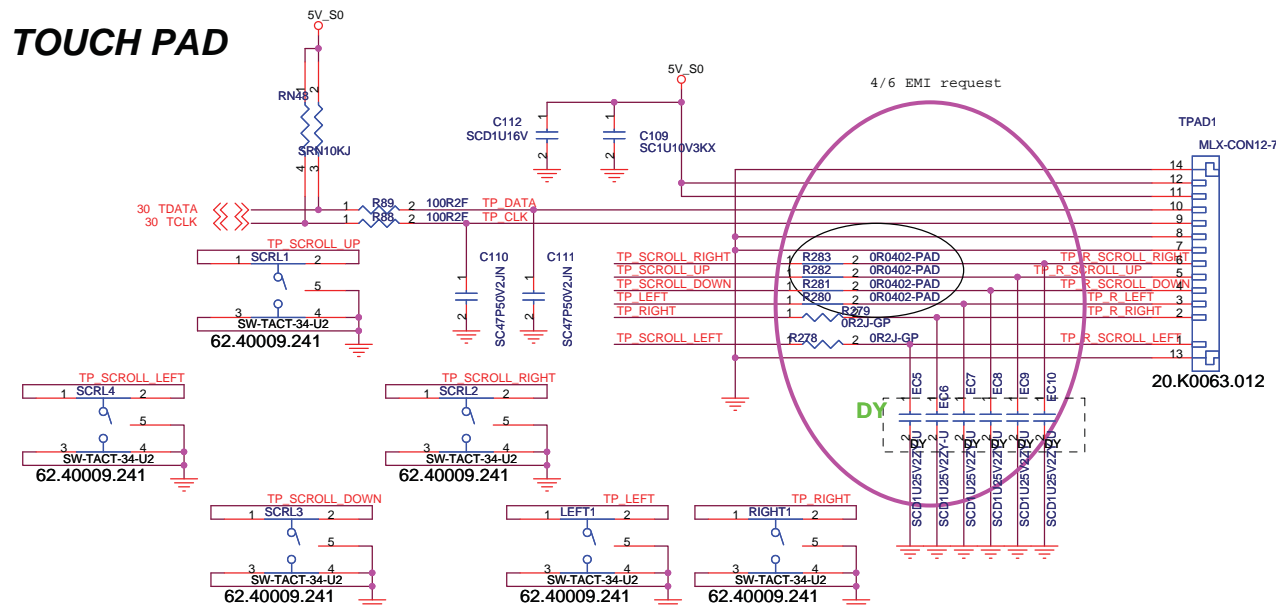
P4 BUTTON

P5 BUTTON



POWER BUTTON

TOUCH PAD



<Variant Name>

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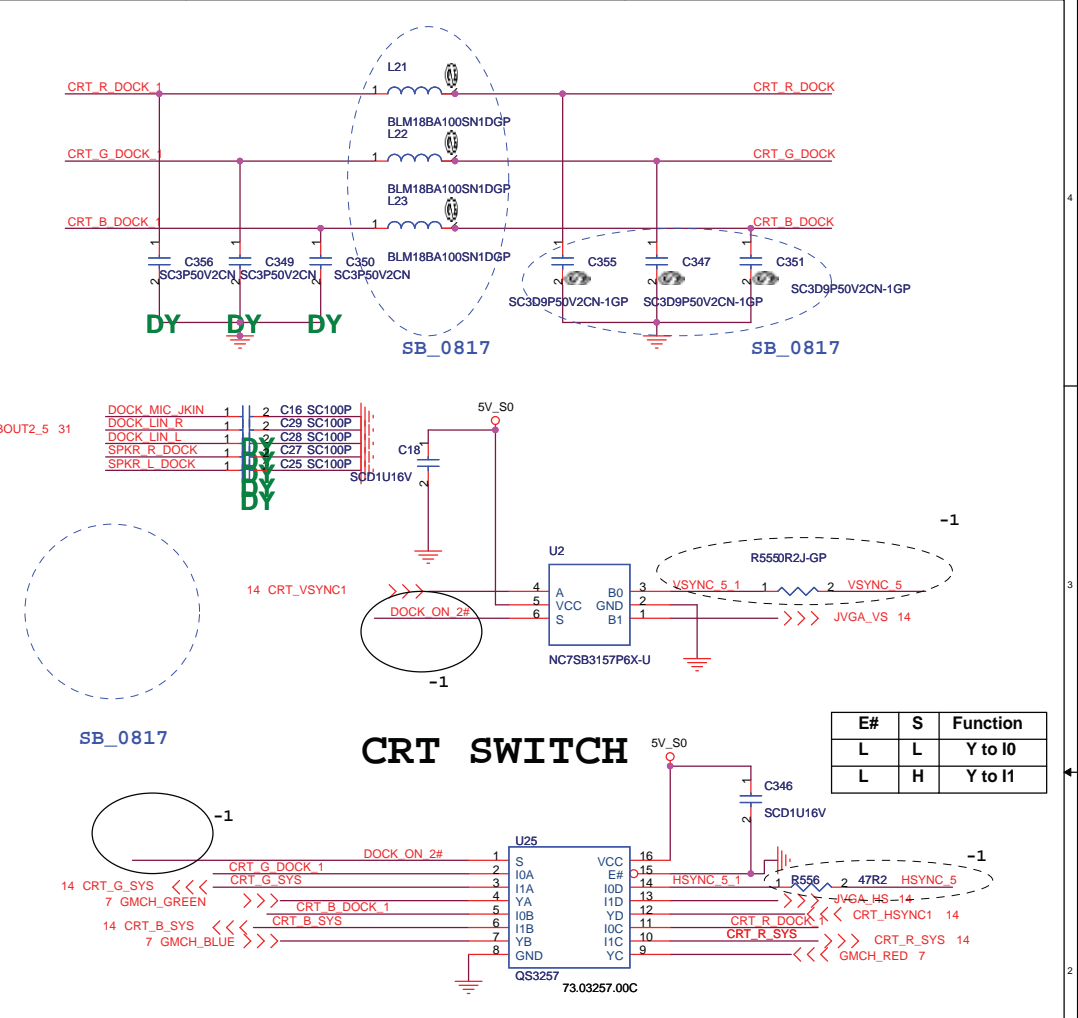
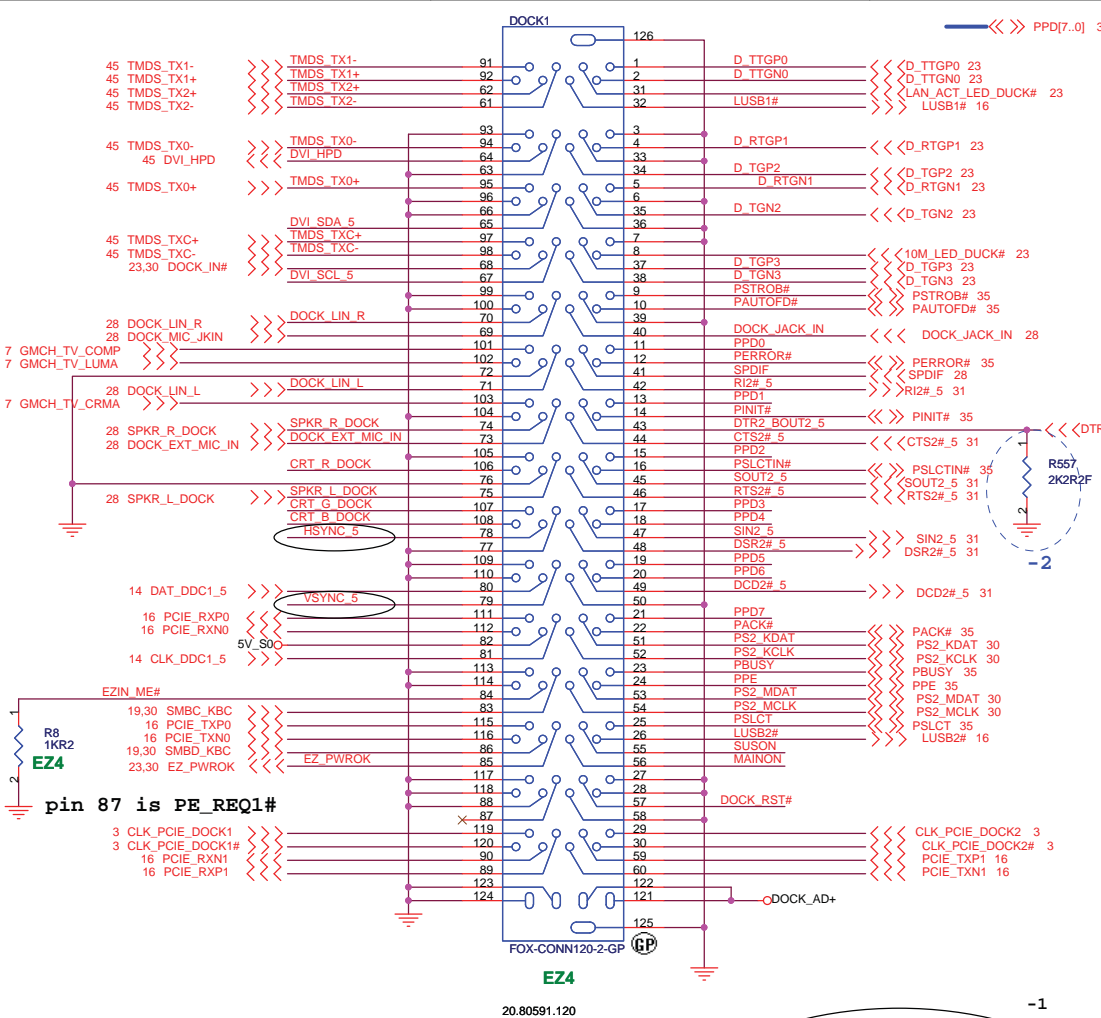
| Title | | | |
|---------------|----------------------------|-------|----------|
| KBC&TPAD CONN | | | |
| Size | Document Number | Rev | |
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iv

SB_0817

| | |
|----------|----------|
| A15 | (B1) |
| A14 | (B2) |
| \vdots | \vdots |
| A2 | (B14) |
| A1 | (B15) |

| | | | |
|-----------------------------|----------------------------|----------------|-----------|
| Title | | | |
| <i>FWH and Debug</i> | | | |
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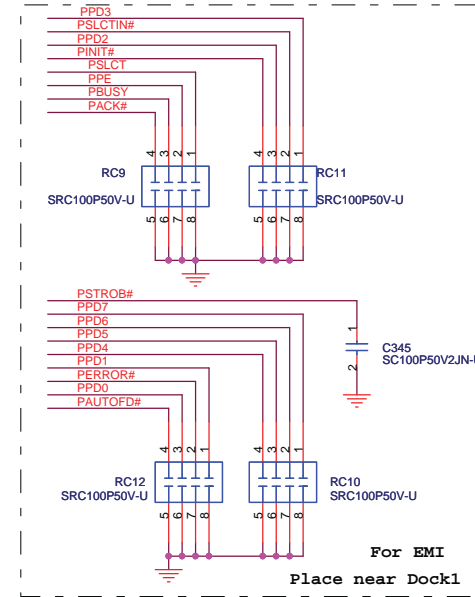
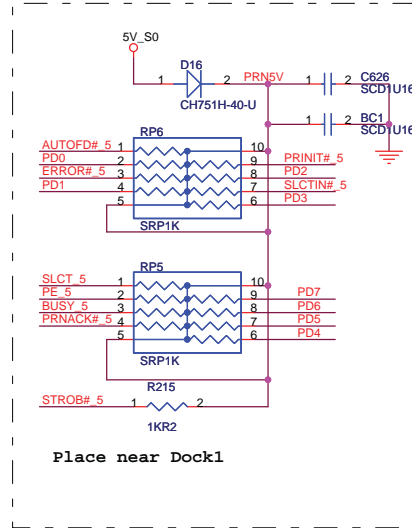
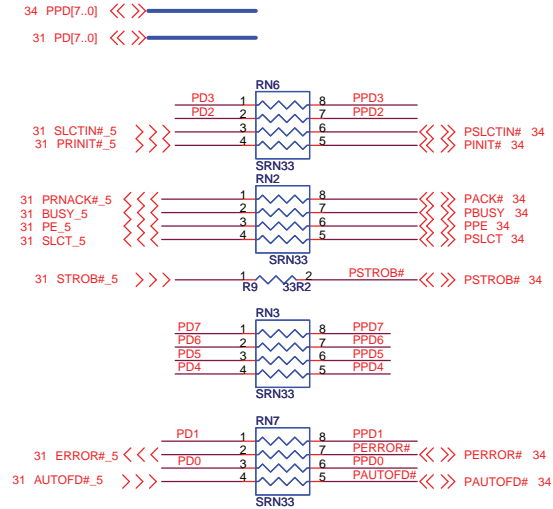


| Function | CRT | TV |
|----------|-----|----|
| SYSTEM | H | H |
| DOCK | L | L |

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PRINT PORT



<Variant Name>

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Title

EASY PORT4 (2/2)

Size
A3

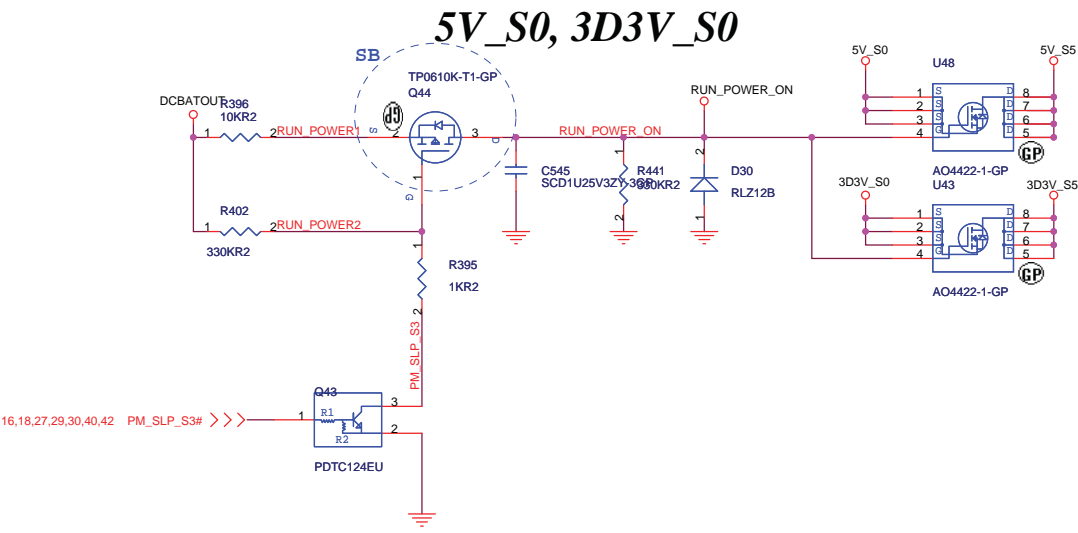
Document Number

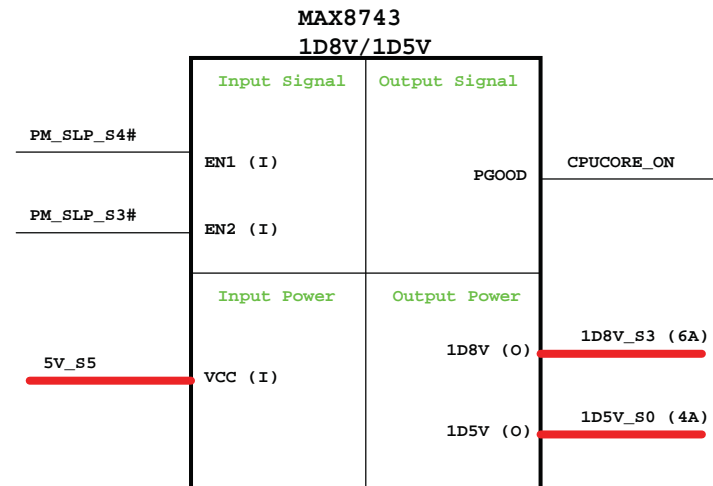
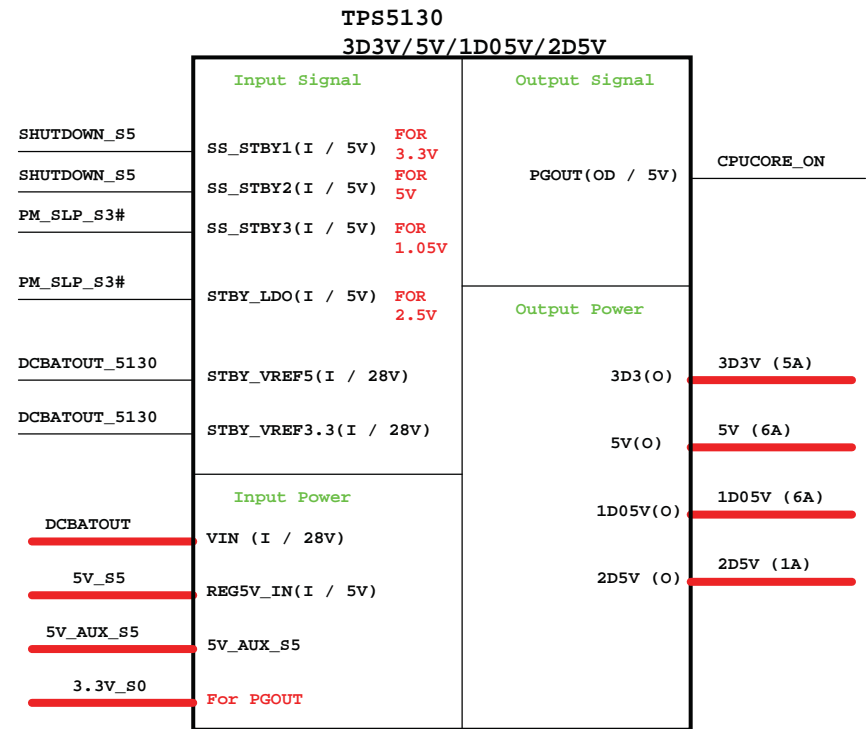
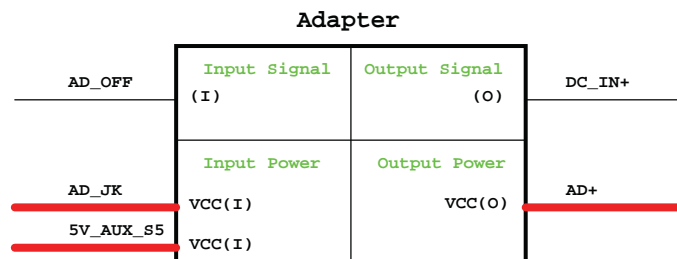
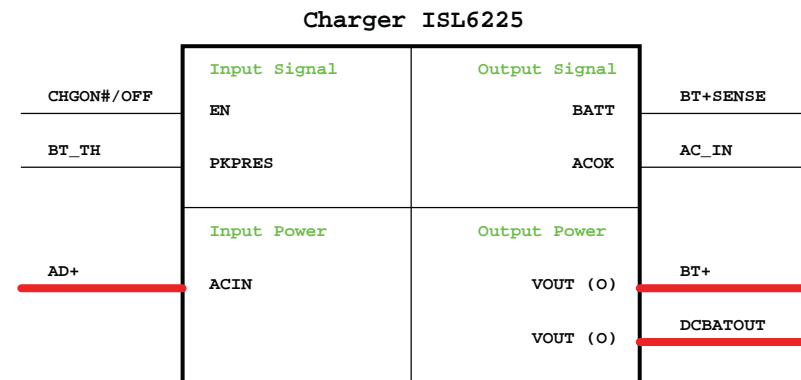
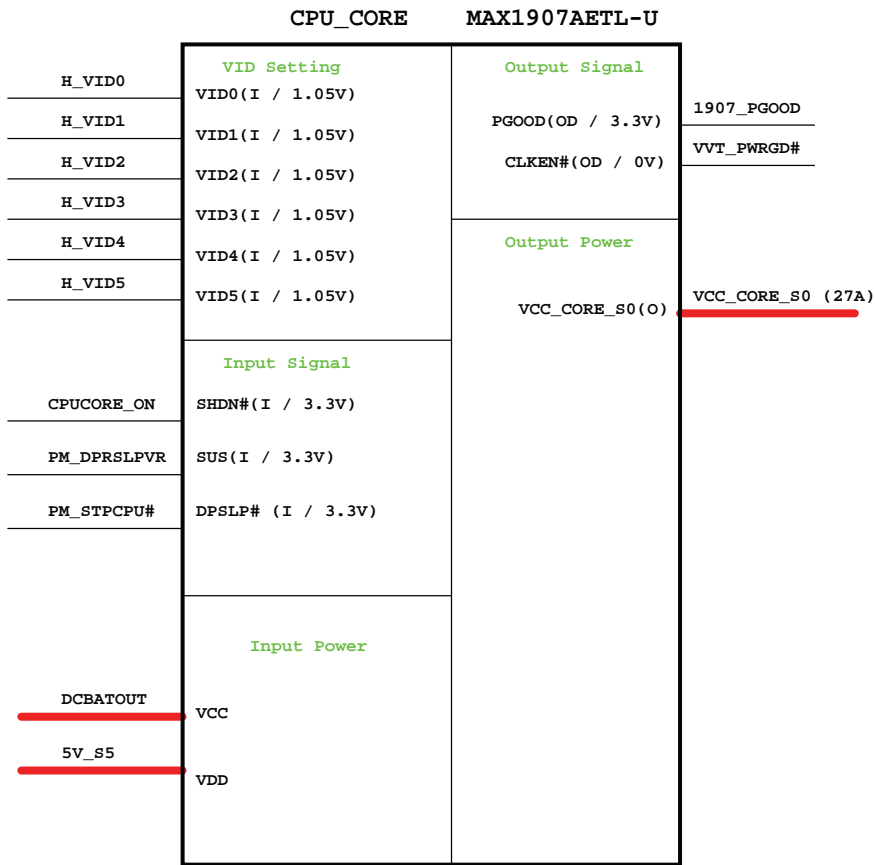
Myna2

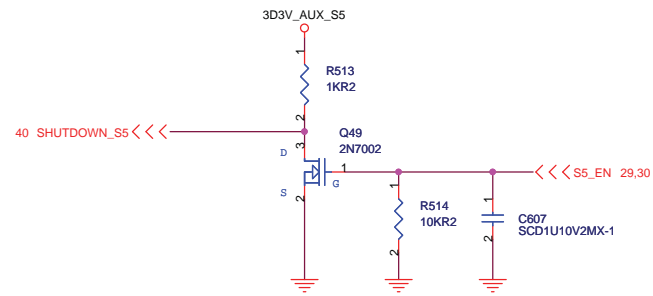
Rev
SB

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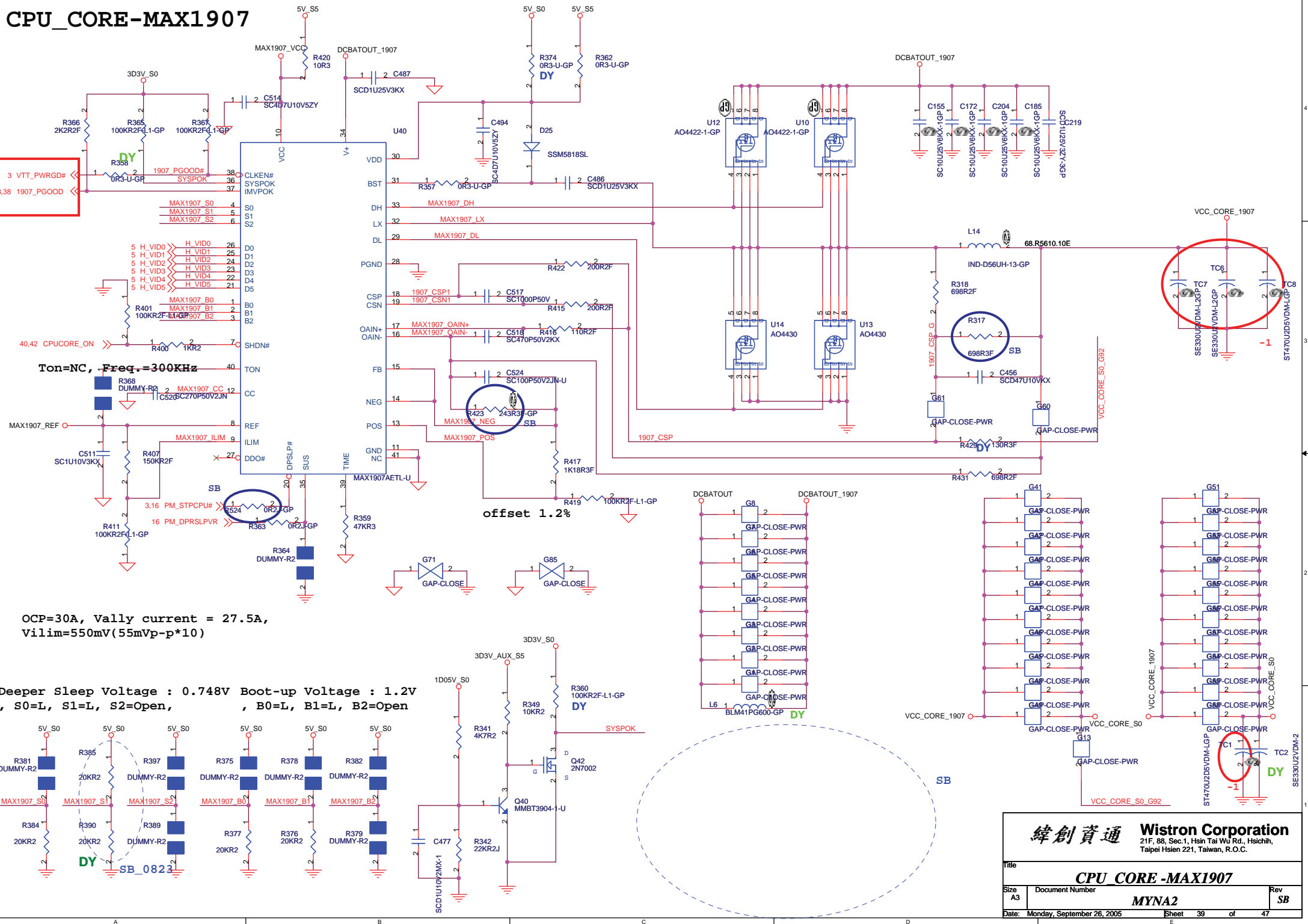




PWRGD for NB and SB



CPU_CORE-MAX1907



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| | |
|-------|---------------------------------|
| Title | <i>CPU_CORE -MAX1907</i> |
|-------|---------------------------------|

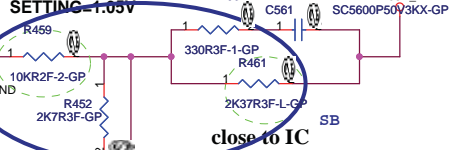
| | | |
|------------|---------------------------------|------------------|
| Size A3 | Document Number MYNA2 | Rev SB |
|------------|---------------------------------|------------------|

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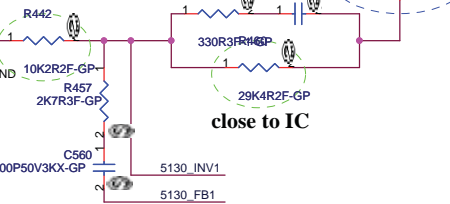
TI TPS5130 for 5V, 3.3V, 1.05V and 2.5V(LDO)

(3D3V=>CH1 , 5V=>CH2 , 1D05V =>CH3)

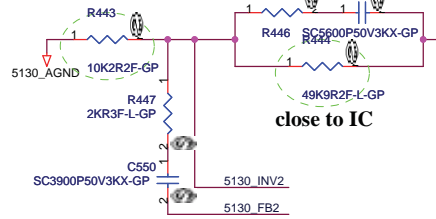
For 1.05V
SETTING=1.05V



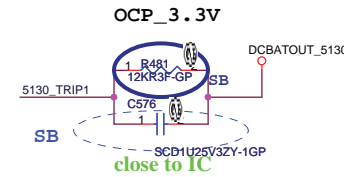
For 3V
SETTING=3.3V



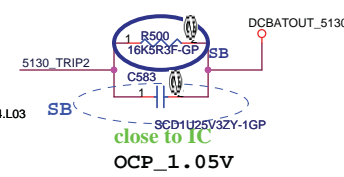
For 5V
SETTING=5.008V



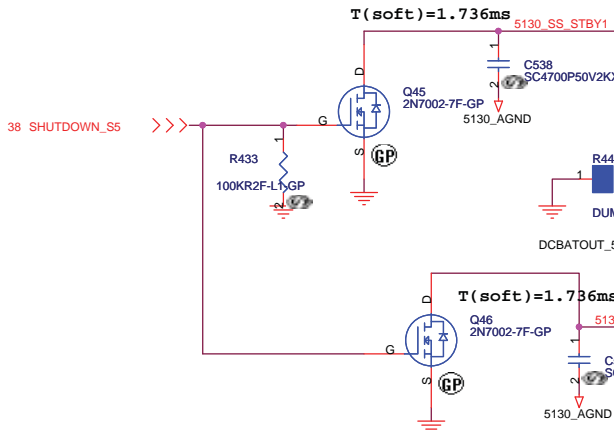
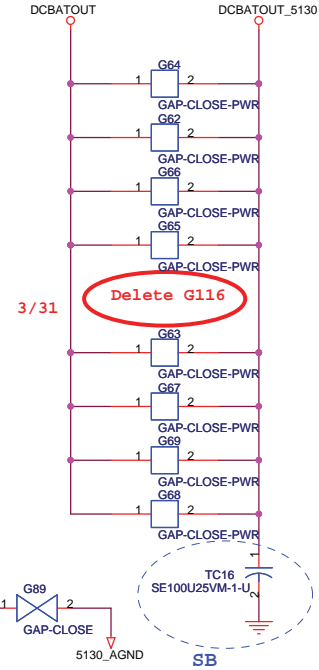
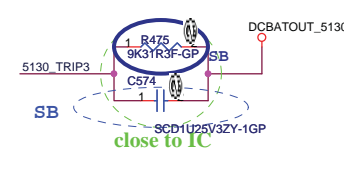
OCP_3.3V



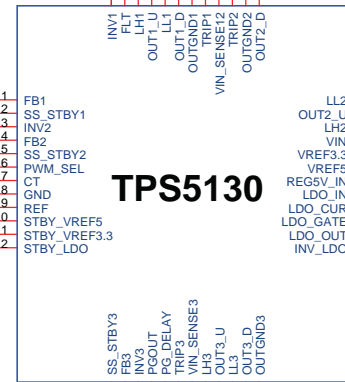
OCP_5V



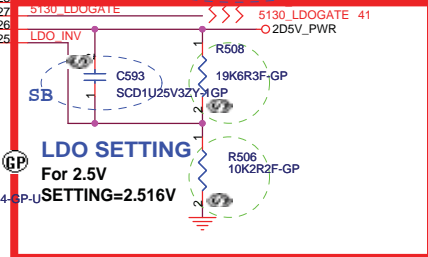
OCP_1.05V



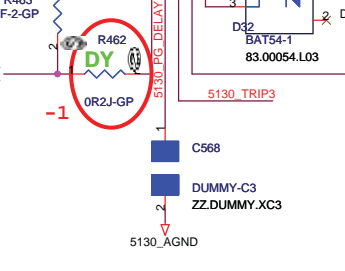
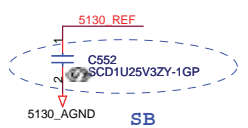
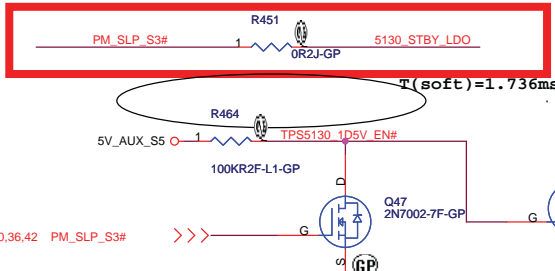
TPS5130



LDO SETTING
For 2.5V
SETTING=2.516V



| Condition | Voltage |
|--------------------------|------------|
| H : Auto PWM/SKIP | 2.2V(Min)~ |
| * L : PWM fixed (300KHz) | ~0.3V(Max) |

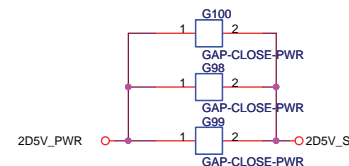
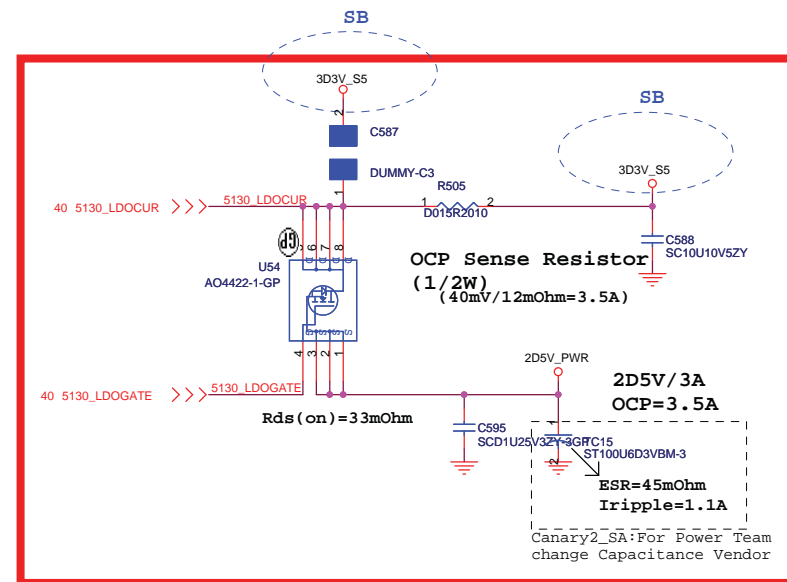
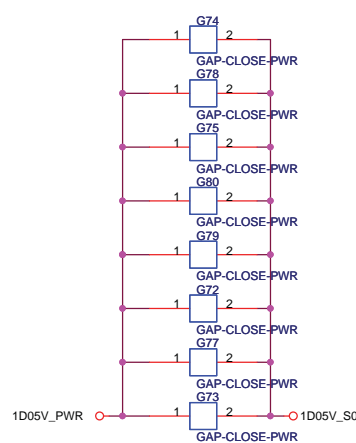
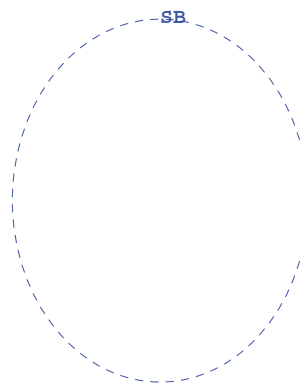
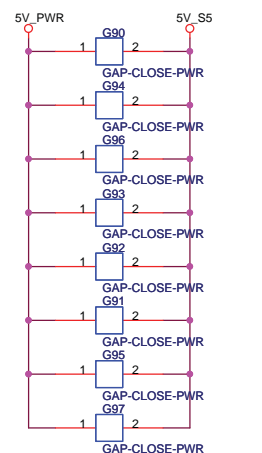


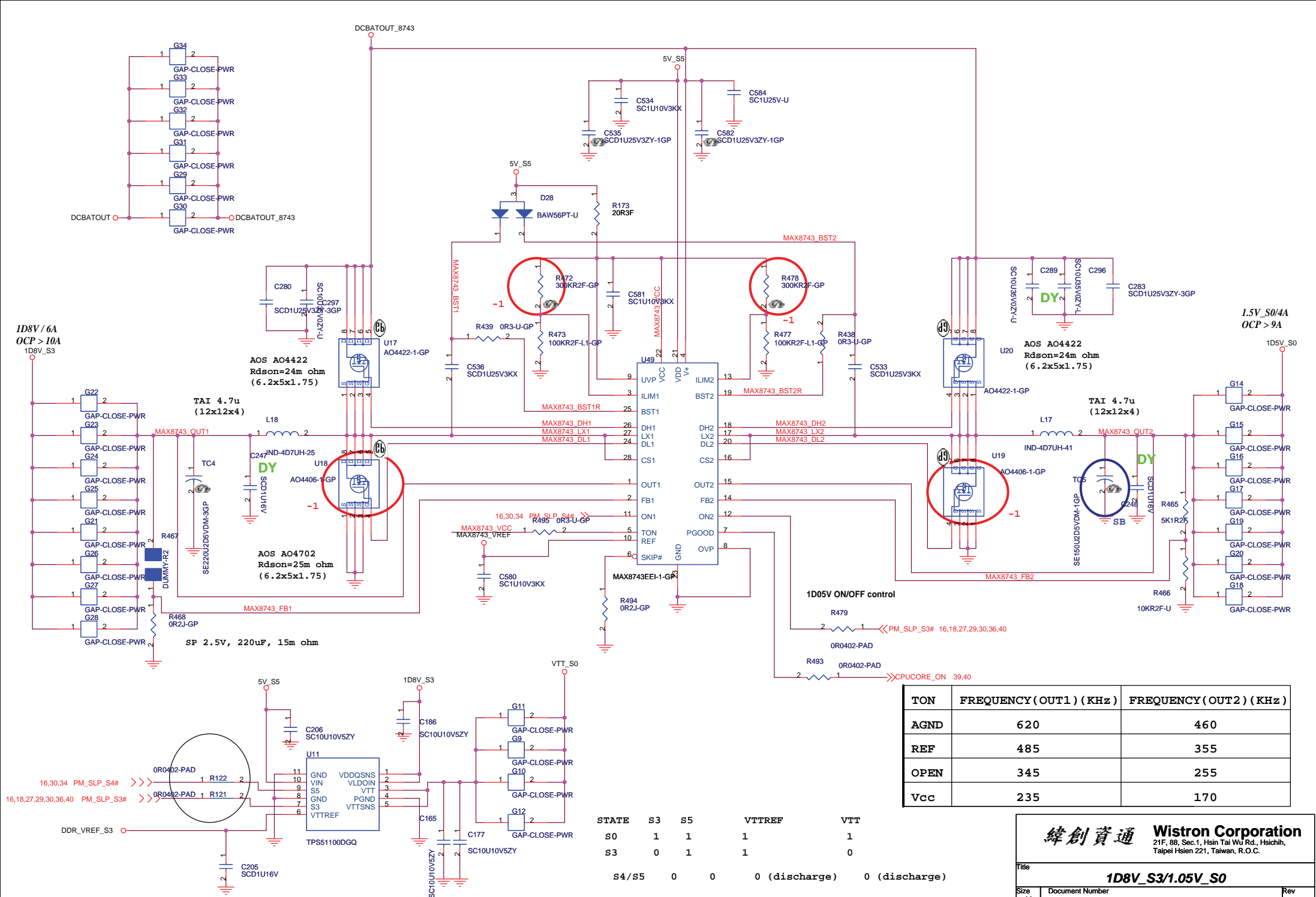
<Variant Name>

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|-------|--------------------------------------|
| Title | TI TPS5130 --- 5V/3.3V/2.5V/1.5(LDO) |
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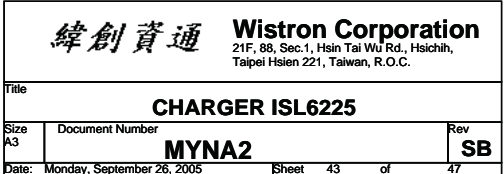
(3D3V=>CH1 , 5V=>CH2 , 1D05V =>CH3)





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 Taipei Hsien 221, Taiwan, R.O.C.

| | | | | | |
|-------|----------------------------|--|------------------|----|-------|
| Title | | | 1D8V_S3/1.05V_S0 | | |
| Size | Document Number | | | | Rev |
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|----------------------------------|-----------------|----|-------|
| Title | | | |
| AD/BAT CONN | | | |
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